Large Current External FET Controller Type Switching Regulator

Step-down, High-efficiency Switching Regulator (Controller type)

BD9040FV, BD9045FV

●Outline

BD9040FV and BD9045FV are 1ch, and 2ch switching controllers that can be used within the wide range of the input. Highly effective can be achieved by the synchronous rectification method and it is possible to contribute to the eco-design of all electronic equipment (energy-saving).

BD9040FV (output type of 1ch synchronous rectification) and BD9045FV (output type of 2ch synchronous rectification)

●Feature（BD9040FV， BD 9045FV）

1) Power-supply voltage：4.5V to 18V
2) Standard voltage 0.9V±1%
3) The overcurrent of timer latch type, excess voltage, short, and RTO/S protection are built-in
4) The switching frequency is changeable.（200kHz to 750kHz）
5) A ceramic capacitor can be used for the output.

●Usage

For thin television, DVD･HDD recorder , STB, amusement and others.

●Absolute maximum rating (Ta=25℃)

Item	Sign	rating	Unit
Power-supply voltage	Vcc	20	V
EN input voltage	V_{EN}	20	V
SW voltage	V_{SW}	Vcc	V
Voltage between BOOT-SW	V_{BOOT}	6	V
Permissible loss 1	Pd1	0.81** (BD9040FV)	W
Permissible loss 2	Pd2	0.94*** (BD9045FV)	W
Range of operating temperature	Topr	-40 to +85	℃
Storage temperature range	Tstg	-55 to +150	℃
Junction temperature	Tjmax	150	℃

** Ta=25℃ or more is reduced with 6.5mW/℃.

*** Ta=25℃ or more is reduced with 7.5mW/℃.

●Operation condition (Ta=-40℃ to +85℃)

Item	Sign	Standard value			Unit
		Minimum	Standard	Maximum	
Power supply voltage***	Vcc	4.5	12	18	V
Timing resistance	RT	39	—	130	kΩ
Frequency of oscillator	Fosc	200	—	750	kHz

*** Please be short-circuited to use VREG5 and VCC when the power-supply voltage is 6V or less.

＊ The radiation design is not done.

Apr.2008

● Electric characteristic (as long as it doesn't specify it Ta=25℃ VCC=12V EN=5V) （BD9040FV）

Item	Sign	Target value			Unit	Condition
		Minimum	Standard	Maximum		
VCC Current of bias	ICC	-	3	6	mA	
Standby current	ISTB	-	430	860	μA	V_{EN}=0V
［VREG5］						
Standard voltage output voltage	VREG5	5	5.5	6	V	
Load stability level	VREG5_L	-	20	50	mV	IV_{REG5}=0 to 6mA
［VREG3 part]						
Standard voltage	VREG3	2.85	3.0	3.15	V	
Load stability level	VREG3_L	-	10	20	mV	IV_{REG3}=0 to 1mA
［prevention part for mis-operation of low input］						
VREG5 Threshold voltage	VREG5_UVLO	3.4	3.8	4.2	V	V_{REG5}:Sweep down
VREG3 Threshold voltage	VREG3_UVLO	2.4	2.5	2.6	V	V_{REG3}:Sweep down
［Oscillator］						
Oscillation frequency	FOSC	240	300	360	kHz	RT=91 kΩ
［Error amplifier］						
VO input bias current	Ivo+	-	-	1	uA	
Source current	Isource	-12	-6.5	-2	mA	V_{FB}=1.1V
Sink current	Isink	0.75	1.5	5	mA	V_{FB}=0.7V
Return standard voltage	VOB	0.891	0.900	0.909	V	FB-COMP Short
Output short detection voltage	Vosh	0.37	0.45	0.53	V	V_{FB}:Sweep down
Hysteresis voltage	ΔVosh	22	45	90	mV	V_{FB}:Sweep up
［Soft start part］						
Charge current	ISS	-14	-10	-6	uA	Vss=1V
Discharge current 1	IDIS	0.6	1.7	5	mA	Vss=1V
Discharge current 2	IDIS2	2.35	3.3	4.62		Vss=1V, VEN_SS=0V
Maximum voltage	Vss_MAX	1.75	1.95	2.15	V	
Standby current	Vss_STB	-	-	0.3	V	
［overcurrent protection Division］						
CL inflow current	Iswin	9	10	11	uA	V_{CL}=Vcc-0.2V
［Overvoltage protection Division］						
Detection voltage	Vovp	1.06	1.1	1.14	V	
［Timer latch circuit Division］						
Source current	ITM	-14	-10	-6	uA	V_{TM}=1V
Threshold voltage	Vth_TM	0.9	1	1.1	V	
OFF Sink current	IOFFS	0.6	1.7	5	mA	V_{TM}=0.5V
［Each ch control part］						
EN pull-up resistor	R_{EN}	150	300	450	kΩ	
EN_SS pull-up resistor	R_{EN_SS}	150	300	450	kΩ	

Reference data (as long as it doesn't specify it Ta=25℃)

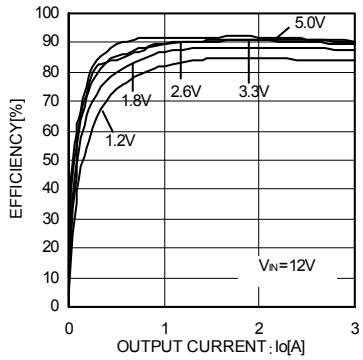


Fig.1 Efficiency 1

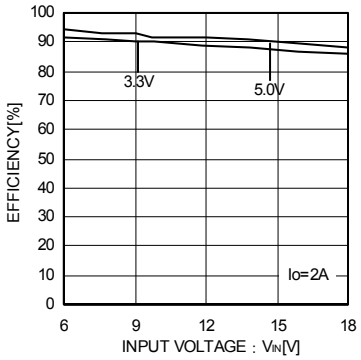


Fig.2 Efficiency 2

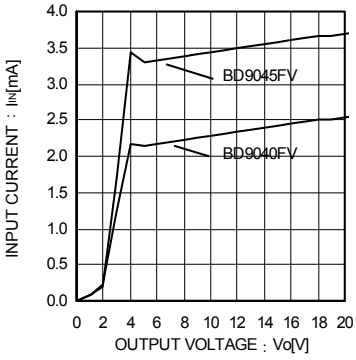


Fig.3 Circuit current

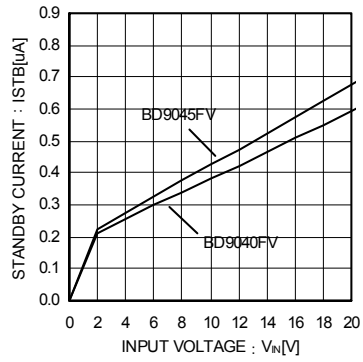


Fig.4 Standby current

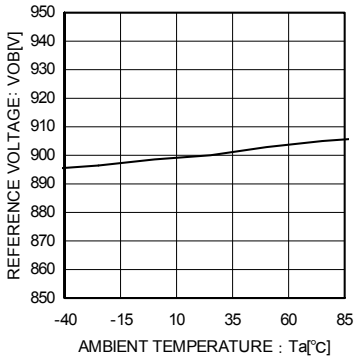


Fig.5 Standard voltage temperature characteristic

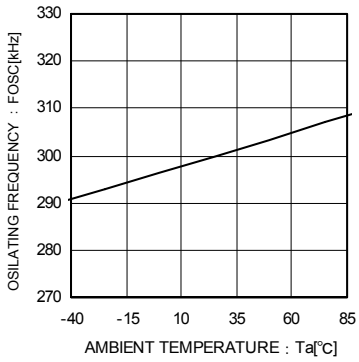


Fig.6 Frequency temperature characteristic

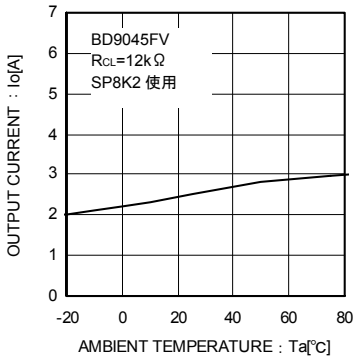


Fig.7 Overcurrent protection temperature characteristic

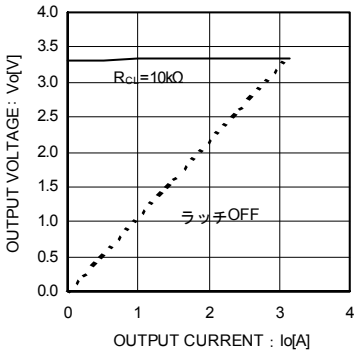


Fig.8 Loading regulation

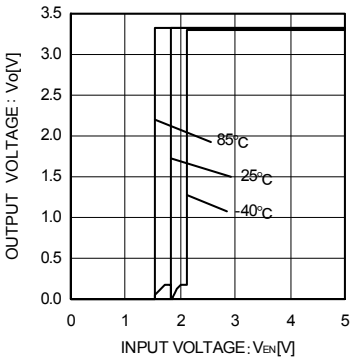


Fig9. EN Threshold voltage

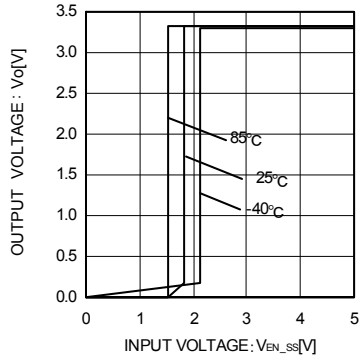


Fig.10 EN_SS Threshold voltage

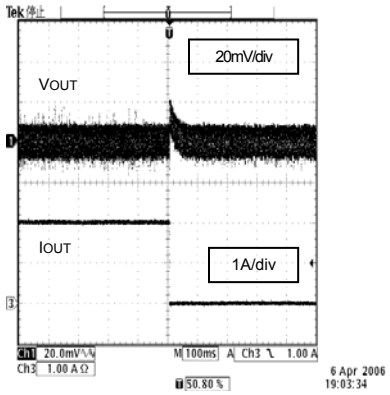


Fig.11 Load response1

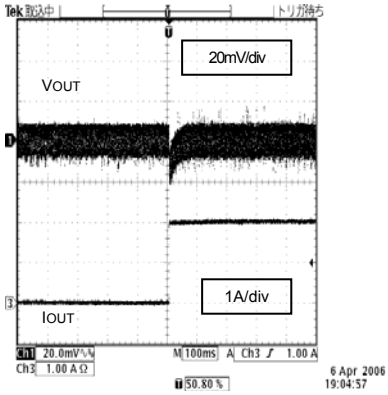
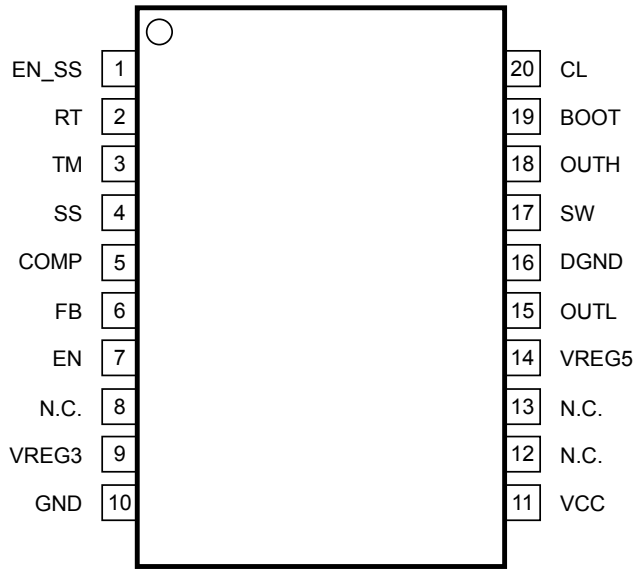


Fig.12 Load response 2

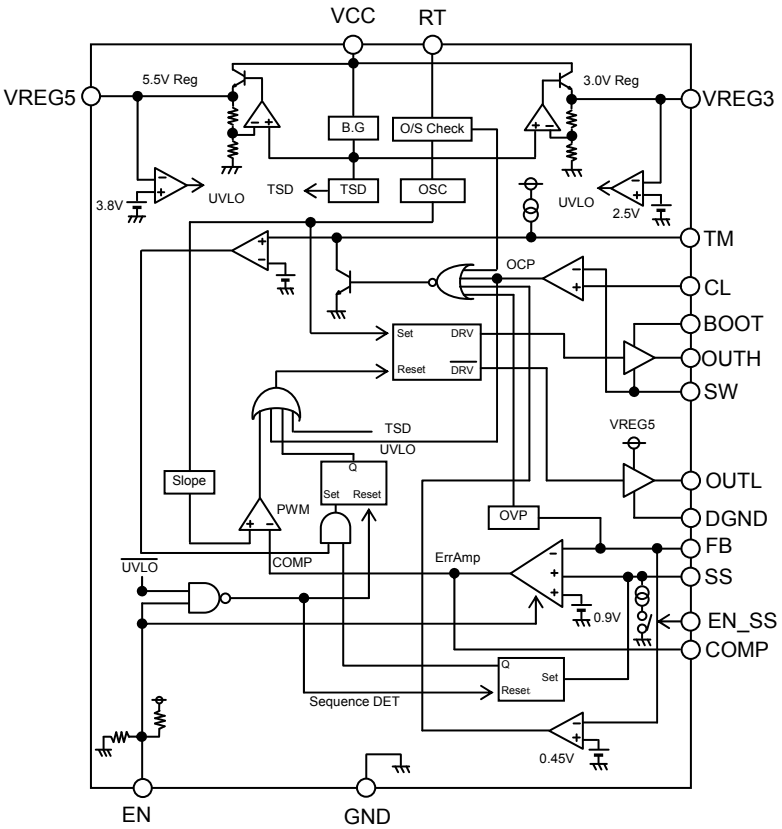
○ Pin distribution chart



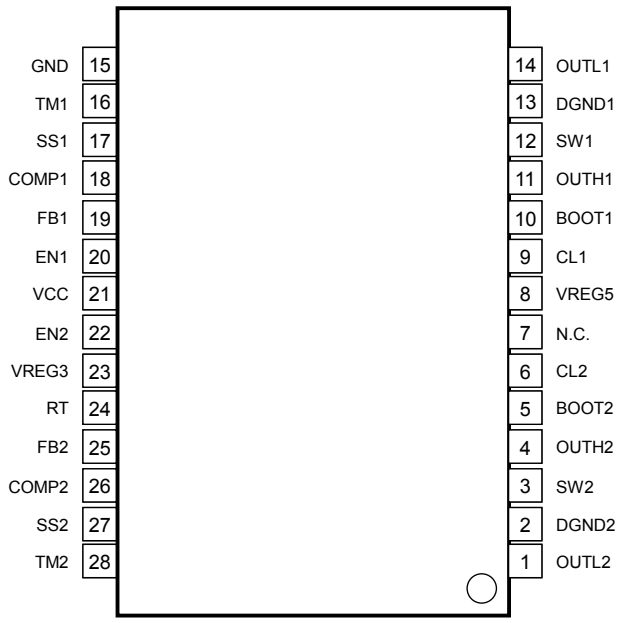
○Terminal number and terminal name

Terminal number	terminal name	Function
1	EN_SS	SS discharge Delay ON/OFF terminal
2	RT	Oscillation frequency setting terminal
3	TM	Output OCP and OVP timer latch setting terminal
4	SS	Soft start time setting terminal
5	COMP	Error amplifier output
6	FB	Error amplifier input
7	EN	Output ON/OFF terminal
8	N.C	Unconnected terminal
9	VREG3	REG output for standard power supply
10	GND	GND
11	VCC	Input power supply terminal
12	N.C	Unconnected terminal
13	N.C	Unconnected terminal
14	VREG5	REG output for FET drive
15	OUTL	drive terminal at low side of FET gate
16	DGND	Source terminal at low side of FET
17	SW	High side FET source terminal
18	OUTH	Terminal of drive at high side in FET gate
19	BOOT	OUTH driver power supply terminal
20	CL	Overcurrent detection setting terminal

○Block chart



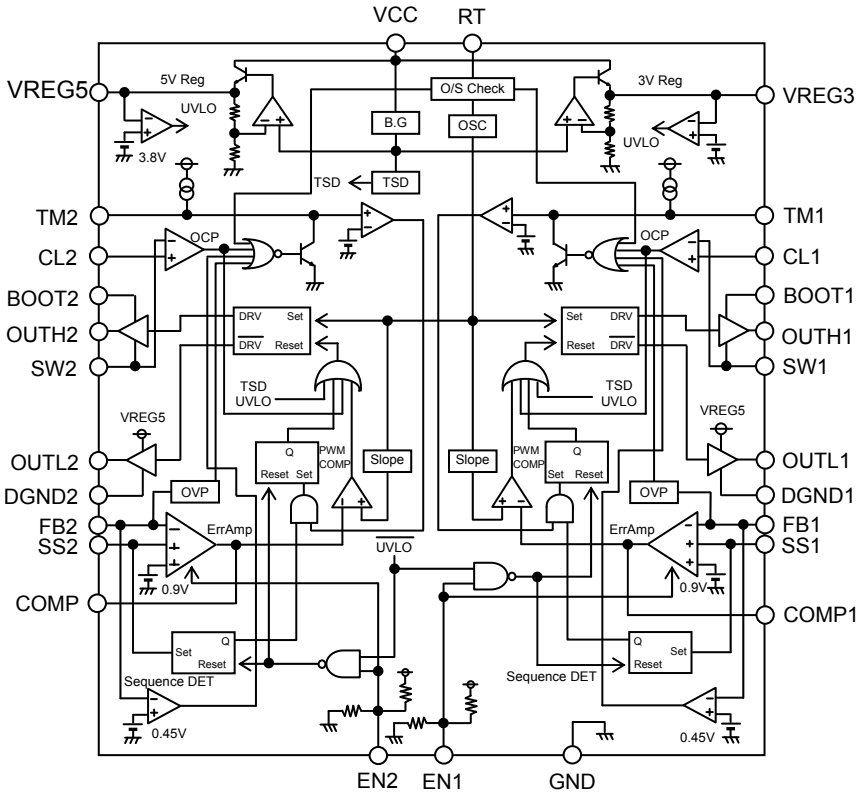
○Pin distribution chart



○Terminal number and terminal name

Terminal number	terminal name	Functions
1	OUTL2	Terminal 2 of drive at low side FET gate
2	DGND2	Low side FET source terminal2
3	SW2	High side FET source terminal2
4	OUTH2	Terminal 2of drive at high side of FET gate
5	BOOT2	OUTH2 driver power supply terminal
6	CL2	Overcurrent detection setting terminal 2
7	N.C.	Unconnected terminal
8	VREG5	REG output for FET drive
9	CL1	Overcurrent detection setting terminal 1
10	BOOT1	OUTH1 driver power supply terminal
11	OUTH1	Terminal 1of drive at high side of FET gate
12	SW1	High side FET source terminal 1
13	DGND1	Low side FET source terminal 1
14	OUTL1	Terminal 1of drive at low side of FET gate
15	GND	GND terminal
16	TM1	Output 1 OCP and OVP timer latch setting terminal
17	SS1	Soft start time setting terminal 1
18	COMP1	Error amplifier output 1
19	FB1	Error amplifier input1
20	EN1	Outpt1ON/OFF terminal
21	VCC	Input power supply terminal
22	EN2	Output2ON/OFFterminal
23	VREG3	REG output for standard power supply
24	RT	Oscillation frequency setting terminal
25	FB2	Error amplifier input 2
26	COMP2	Error amplifier output 2
27	SS2	Soft start time setting terminal 2
28	TM2	Output 2 OCP and OVP timer latch setting terminal

○Block chart



○ Operational description of each block

・Error amplifier（ErrAmp）

It is a circuit to compare the 0.9V reference voltage and the output voltage's feedback voltage. Switching Duty is determined by the COMP voltage that is the result of the comparison. In addition, due to the SS terminal voltage on start-up, the Soft Start begins operating, and so the COMP voltage is limited by the SS voltage.

・Oscillator（OSC）

It is a block, the oscillating frequency of which is decided by RT and can be set up to 200kHz~750kHz.

・SLOPE

It is a block in which triangular wave is created from the clock generated by the OSC. And the generated triangular wave is transmitted to the PWM comparator.

・PWM Comparator（PWM COMP）

The error amplifier's output COMP voltage and the SLOPE block's triangular wave are compared, and the switching Duty is determined. The switching duty is limited by the maximum Duty ratio internally decided and can not become 100%.

・Reference voltage（5V Reg, 3V Reg）

It is a block to generate 5.5V and 3V internal reference voltage.

・Overcurrent protection circuit（OCP）

At the time of OUTH=H, if SW voltage becomes not more than CL voltage, the overcurrent protection circuit operates. When the overcurrent protection operates, the Duty is limited, and so the output voltage is lowered. Moreover, when an overcurrent is detected by the overcurrent protection circuit, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.

・Overvoltage protection circuit（OVP）

When FB voltage becomes more than 1.1 V, the overvoltage protection operates. When the overvoltage protection operates, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.

・Output short circuit protection circuit

If FB voltage becomes not more than 0.4V, the output short circuit protection circuit operates. When the output short circuit protection operates, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.

・O/S　Check

When RT terminals become open or short circuit states, RT OPEN and SHORT circuit protections operate respectively.
When RT terminals' open or short circuit state is detected, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.

・Under Voltage Lockout (UVLO) / Thermal Shutdown（TSD）

When VREG5 becomes no more than around 3.8V or VREG3 no more than around 2.5, the output of the under voltage lockout is turned off.
Then, When VREG5 becomes more than around 4.2V or VREG3 more than around 2.6, the output of the under voltage lockout is reset.
Moreover, when the temperature of chip becomes more than around 150□, the output of the thermal shutdown (TSD) is turned off, and when it is returned to a certain temperature, the output is reset.
When UVLO and TSD operate, the capacitors of TM and SS are discharged.

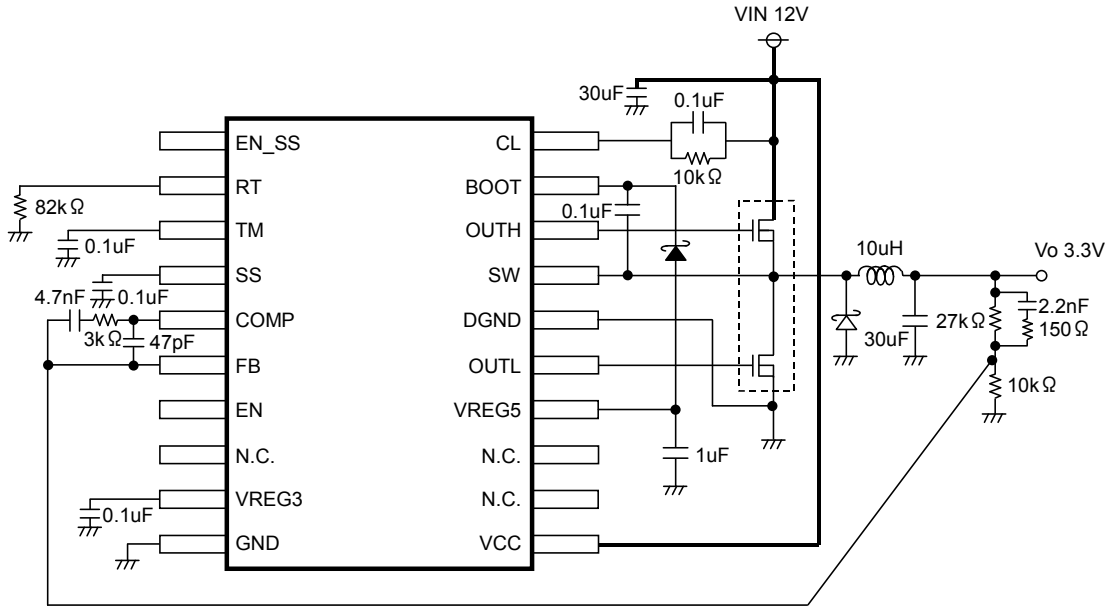
・Function of EN

EN is pulled down in regard to GND and pulled up in regard to VCC, and normally EN=H.
At the time of EN=L, the capacitors of OFF, TM and SS of output are discharged, and become the standby state.
(As for BD9045FV, due to EN1 and EN2, the capacitors of OFF, TM and SS of each ch output are discharged. In addition it becomes the standby state when both EN1 and EN2 are made to be L).

・Function of EN_SS（BD9040FV alone）

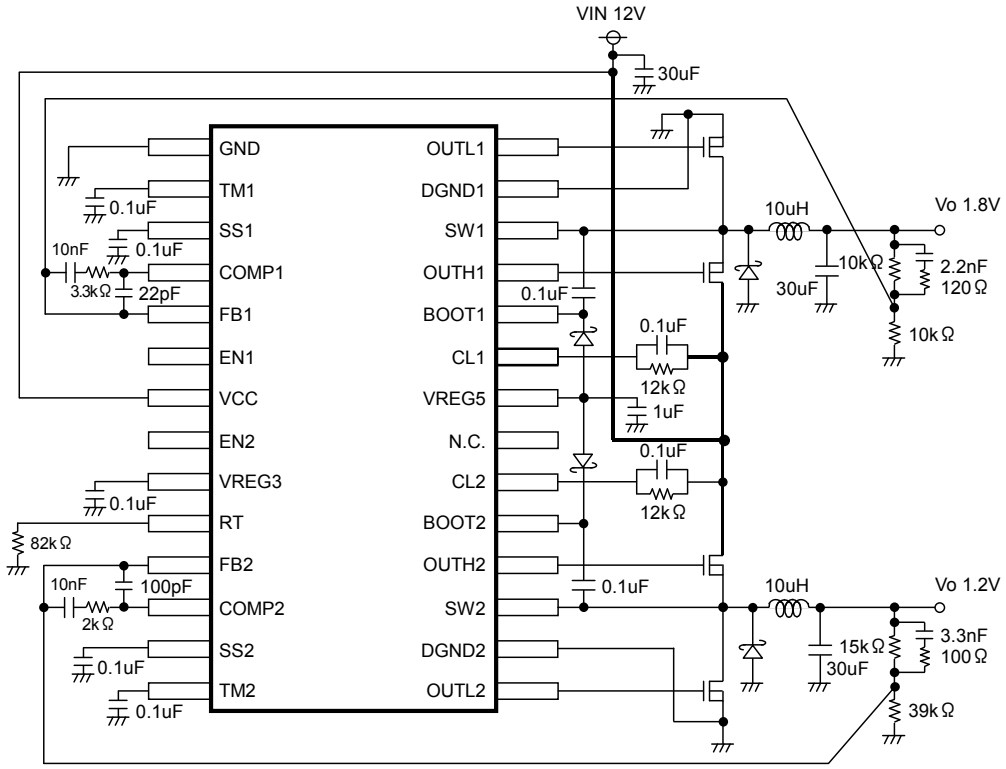
EN_SS is pulled down in regard to GND and pulled up in regard to VCC, and normally EN_SS=H.
At the time of EN_SS=L, the capacitors of OFF, TM and SS of output are discharged.
At the time of EN_SS=L, the capacitor of SS is constant-current discharged, so it can be made delayed during output's OFF.

BD9040FV



These characteristics vary with the layout of board and the kind of parts etc, so please confirm them thoroughly with actual devices.

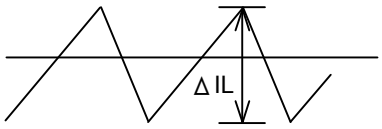
BD9045FV



These characteristics vary with the layout of board and the kind of parts etc, so please confirm them thoroughly with actual devices.

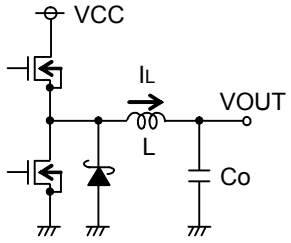
● Method to select the application parts

(1) Setting of output L constant



The value of coil has a great influence on output ripple current. As shown in the formula (1), the bigger the coil, and the higher the switching frequency, the more the ripple current is reduced.

$$\Delta IL = \frac{(VCC\text{-}VOUT) \times VOUT}{L \times VCC \times f} \quad [A] \cdots (1)$$



Output ripple current

The appropriate set value of output ripple current is about 30% of maximum output current.

$\Delta IL = 0.3 \times IOUTmax.[A] \cdots (2)$

$$L = \frac{(VCC\text{-}VOUT) \times VOUT}{\Delta IL \times VCC \times f} \quad [H] \cdots (3)$$

(ΔIL : output ripple current, f : switching frequency)

□ If a current exceeding the rated current value of coil flows in coil, the coil will cause magnetic saturation, and so the efficiency is reduced.

Please select in such a way that a good margin is left so that the peak current does not exceed the coil's rated current value.

□ Please select such a coil as has a low resistance component in order to reduce the loss in the coil and improve the efficiency.

(2) Setting of output constant Co

Please select the larger capacitance from between the allowable value of ripple voltage V_{PP} and the allowable value of drop voltage at a sudden change of load, as the value of the capacitor used on the output. The output ripple voltage is determined by the following formula.

Drop of voltage: $$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{Co} \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [V] \cdots (4)$$ provided that f : switching frequency

Please set in such a way that the ripple voltage is within the allowable one.

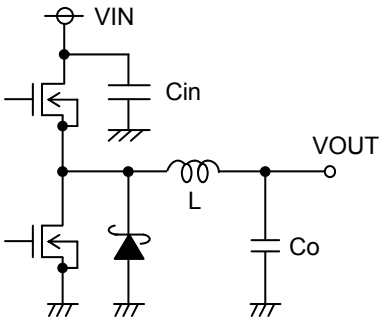
□ Please select the rating of capacitor in such a way that a good margin is left for output voltage. If ESR is small, the output ripple voltage can be reduced. Moreover, because it is necessary to set the initial rise time of output within the soft start time, please also take the conditions of the formula (5) into consideration while determining the capacitance of the output capacitor.

$$Co \leqq \frac{Tss \times (ILimit - I_{OUT})}{V_{OUT}} \quad \cdots (5)$$

Tss : soft start time
I_{OUT} : load current
V_{OUT} : output voltage
ILimit : detected value of overcurrent Refer to

If the capacitance is not the optimum, it is possible to cause bad start-up etc.

(3) Selection of input capacitor (Cin)



Input capacitor

Input capacitor plays a role in reducing the output impedance of the power supp connected on input terminal (VCC). If this power supply's output impedance increases, the input voltage (VCC) becomes unstable, and the deterioration of oscillation or ripple rejection characteristics may be caused. Therefore, please be sure to put it near VCC and GND terminals.

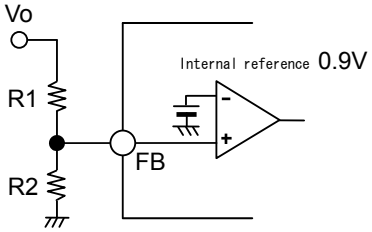
It is necessary to select the input capacitor with low ESR and small capacitance change caused by temperature change so as to make full preparation for big ripple current. The ripple current IRMS is determined by the formula (Io).

$$IRMS = IOUT \times \frac{\sqrt{VOUT\ (VCC - VOUT)}}{VCC} \quad [A] \cdots (6)$$

Moreover, it is greatly dependant on the characteristics of the power supply used on input, the wiring pattern of board and the gate – drain capacitance of MOSFET, so please fully confirm the service temperature, load range and MOSFET's conditions.

(4) Design of feedback resistance constant

Please refer to the following formula for design of feedback resistance. The 1kΩ~330kΩ is recommended as its setting range. If it is no more than 1kΩ, drop in electric power efficiency will be caused. Moreover, if more than 330kΩ is set, the offset voltage becomes large due to the internal error amplifier's input bias current of 0.4uA.

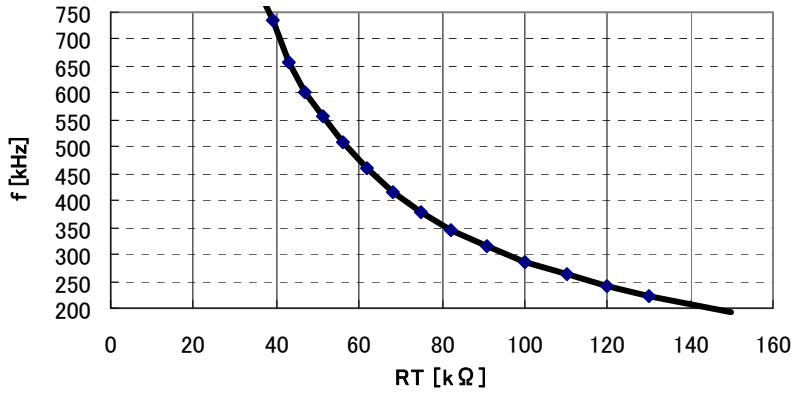


$$Vo = \frac{R1 + R2}{R2} \times 0.9\,[V] \quad \cdots (7)$$

(5) Setting of oscillating frequency

Triangular wave oscillating frequency can be set by connecting a resistor to RT pin. RT determines the currents of charging & discharging the internal capacitor, and the frequency changes. Please refer to the following diagram for setting of the resistance of RT.

If setting is off the range of the following diagram, the switching may stop, and so normal operation can not be ensured, therefore please be careful.



(6) Setting of soft start time

The soft start is necessary for preventing the excessive increase of coil current at the time of start-up and the overshoot at the time of start-up of output voltage. The calculating formula for capacitor & soft start time is shown in the formula (8).

$$T_{SL} = 0.8 \times \frac{Css}{Iss\ (10uA\ typ)}\ [sec] \qquad T_{SH} = 0.7 \times \frac{Vo}{Vcc} \times \frac{Css}{Iss\ (10uA\ typ)}\ [sec] \quad \cdots (8)$$

If the capacitance value is reduced (to no more than 0.01 uF or so), the overshoot in output may be caused.

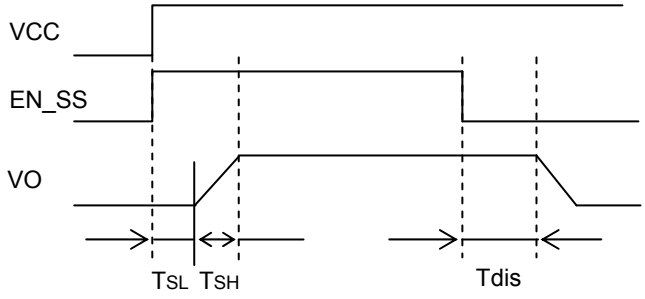
If there is a start-up relation (sequence) with other power supplies, please use high-accuracy parts (x5R) etc.

Still more, the soft start time & waveform vary with input voltage, output voltage, load, coil, output capacitance and phase compensation constant etc, so please confirm with actual devices.

(7) Setting of EN_SS (output delay function) (in the case of BD9040FV)

If EN_SS is made to be L, the output voltage's OFF time can be made delayed. The calculating formula for delay time is shown in the following formula.

$$TDIS = \left(Vss\_MAX(1.95VTyp) - \left(0.8 + 0.7 \times \frac{Vo}{Vcc}\right) \right) \times \frac{Css}{Idis(3.3uA,Typ)}\ [sec] \quad \cdots (9)$$

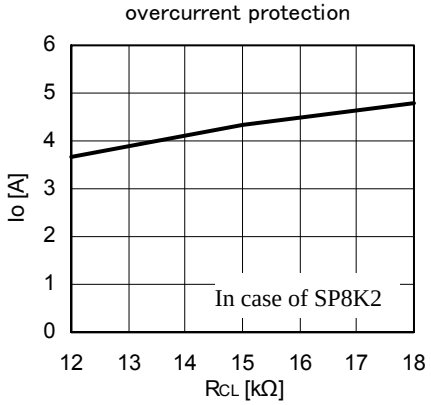


(8) Overcurrent protection

Current limit value (ILimit) is determined by the resistance RCL connected between VCC and CL. (refer to the following diagram)

The current limit is self-feedback type, when overcurrent is detected, the output Duty is reduced, and the current is limited. When load returns to

normal state, the output voltage returns to its former state.



In case of SP8K2

Actual

BD9040FV measurement value of our company's substrate

BD9045FV measurement value of our company's substrate

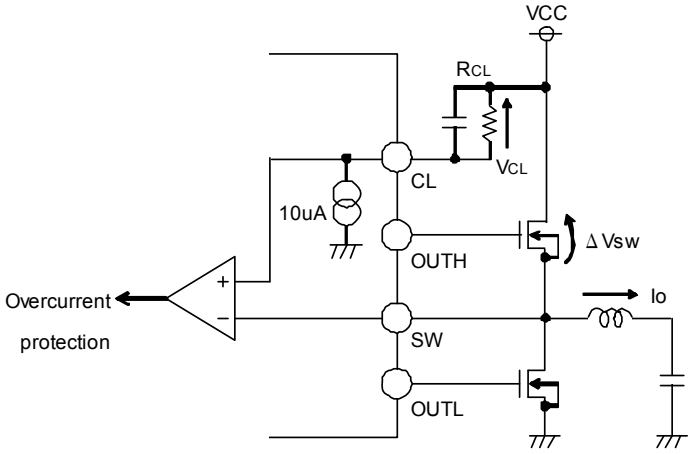
□These values vary with the layout and service condition, so please confirm them thoroughly with actual devices.

Overcurrent protection detection value is dependent on the ON resistance of external FET and so varies with temperature. (Refer to Fig.7 on page 3)

Please determine it in such a way that a good margin is left while setting it. Moreover, in case of different layout of substrate or large gate capacitance of external FET, sufficient voltage between gate and source of external FET can not be provided, the ON resistance becomes high, and so the overcurrent protection value may be greatly changed.

Please use a FET, the gate capacitance of which is no more than1500pF, as external FET. (the recommended: SP8K2, SP8K1)

However, these values vary with the layout and service condition, so please confirm them thoroughly with actual devices.



Compare the V_{CL} that is set by R_{CL} and the ΔVsw that Is generated by ON resistance of loxFET.

(9) Setting of OFF latch timer time

・OFF latch timer is charged if one of the following conditions is met.

- ・Current limit is operating.
- ・Overvoltage protection（FB□1.1V）is operating.
- ・Output short circuit protection（FB□0.45V）is operating.
- ・Resistor connected on RT terminal becomes open.
- ・RT terminal is shorted with GND.
- ・Resistor connected on CL terminal becomes open.

If the charging is started and continued until the fully-charged, the output is OFF latched. The time from start-up of charging till output OFF is determined by the following formula.

$$T_{TM} = \frac{C_{TM}}{I_{TM}\ (10uA\ typ)} \quad [sec] \quad \cdot\cdot\cdot (10)$$

This OFF latch is released once EN is made to be「L」or if VCC is once lowered and then rises again.

(10) Method to set the phase compensation

・Stable condition of application

Shown as below are the stable conditions of the feedback system for negative feedback to return.

・The phase delay when the gain is 1(0dB) is no more than150°（i.e. phase margin is more than 30°）

Two output high frequency step-down switching regulator

Moreover, for DC/DC converter application, because it is sampled by switching frequency, the whole series of GBW are to be set at 1/10 of switching frequency. To sum up, the features aiming at application are as follows.

・The phase delay when the gain is 1(0dB) is no more than150°（i.e. phase margin is more than 30°）

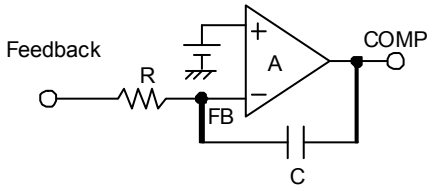
・GBW（i.e. frequency of 0dB gain）at that time is no more than 1/10 of switching frequency

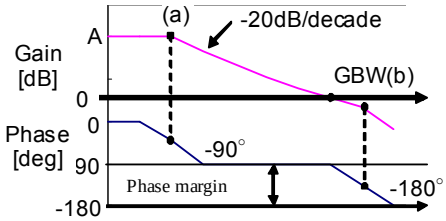
Therefore, it is necessary to raise the switching frequency up to higher frequency in order to raise the response by means of limit of GBW.

The key to ensuring the stability by means of phase compensation is that the quadratic phase delay (-180°) produced by LC resonance is cancelled by quadratic phase lead (i.e. let two phase leads into).

Moreover, GBW (the frequency at the time of gain=1) is determined by the phase compensation capacitor attached on the error amplifier, so make (enlarge) the capacitor larger when you want to reduce the GBW.

□ General integrator (low pass filter)　□ Open loop characteristic of integrator





(a)点　$fa = \frac{1}{2\pi RCA}$ 1.25[Hz]・・・(11)

(b)点　$fa = GBW \frac{1}{2\pi RC}$ [Hz]　・・・(12)

Error amplifier becomes a low pass filter because such measures of phase compensation as □ & □ are taken.

In case of DC/DC converter application, R becomes the parallel of feedback resistance.

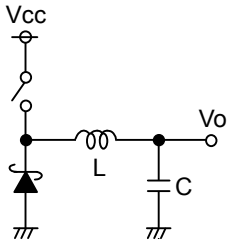
・If output capacitor is aluminum electrolytic capacitor etc, ESR of which is large

If ESR of output capacitor is large (a few Ω), the phase compensation becomes relatively simple. For DC/DC converter application, there is always LC resonance circuit, because of which the phase delay is -180°.

However, if ESR component exists, a phase lead of +90° comes into existence, and so the phase delay becomes -90°. Please set the phase delay within 150°.

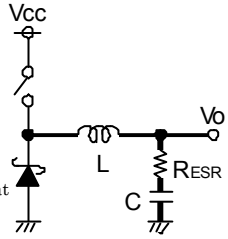
It is a very advantageous means according to circumstances, but as a disadvantage, the ripple component in output voltage increases.

□ LC resonance circuit　□ With ESR



$fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz]・・・(13)

Resonance point phase delay -180° is at



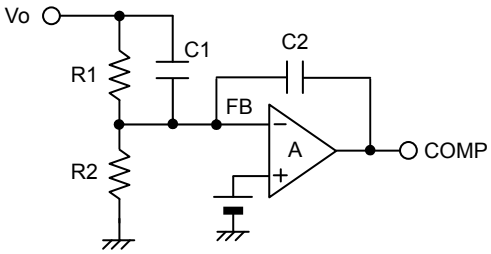
$fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz], resonance point is at this fr ・・(14)

$f_{ESR} = \frac{1}{2\pi R_{ESR}C}$ [Hz], phase lead is at this f_{ESR} (15)

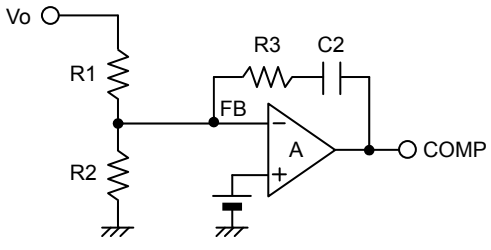
Phase delay -90°

Because of the change of phase characteristic caused by ESR, the phase lead that needs inserting becomes a single one. For this phase lead, please select one of the following.

□ Insert C in feedback resistance　□ Insert R3 in integrator



Phase lead　$fz = \frac{1}{2\pi C1R1}$ [Hz]・・・(16)



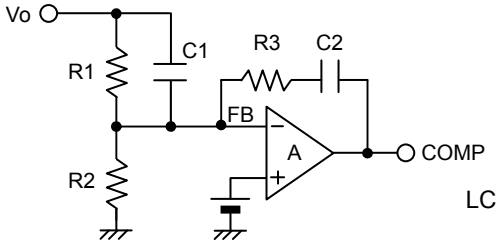
Phase lead　$fz = \frac{1}{2\pi C2R3}$ [Hz]・・・(17)

For setting of the frequency inserting the phase lead, please set it near LC resonance frequency for the purpose of canceling the LC resonance.

・If output capacitor is ceramic capacitor or OS CON etc, ESR of which is small

If an output capacitor, ESR of which is small (a few mΩ), is used in the output, it is necessary to insert two different phase leads from □~□. This is because the phase delay -180° caused by LC resonance appears. As the method of phase compensation, an example shown in □ is given.

□ Phase compensation by means of quadratic phase lead



Phase lead $fz1 = \frac{1}{2\pi R1C1}$ [Hz]・・・(18)

Phase lead $fz2 = \frac{1}{2\pi R3C2}$ [Hz] ・・・(19)

LC resonance frequency $fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz] ・・・(20)

It is the setting of phase lead frequency, for which please insert both near the LC resonance frequency.

Still more, this setting can be easily done and does not need strict calculation etc, so there are some cases where it is necessary to make adjustments with actual devices. Moreover, these characteristics vary with substrates' layouts and load conditions etc, therefore, in case of design of mass production, please confirm them thoroughly with actual devices.

(9) Selection of MOS FET

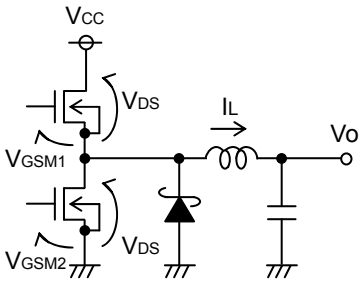


Fig-33

Nch MOS is used as FET.

・V_{DS}＞Vcc ・V_{GSM1}＞voltage between BOOT-SW

・V_{GSM2}＞VREG5

・allowable current＞output current + ripple current

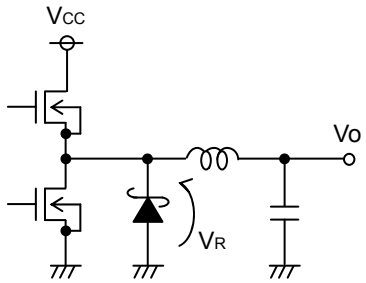
□ More than the set value of overcurrent protection is recommended

□ High efficiency can be achieved if those with small ON resistance are selected.

＊Attention

If the input capacitance of FET is extremely large or it is used with Duty no more than 10%, it is possible that output FETs on both upper side and under side are simultaneously turned on and so the efficiency deteriorates. The input capacitance of output FET is recommended to be no more than 1000pF. But these characteristics vary with substrates' layouts or varieties of parts etc, so please confirm them thoroughly with actual devices when it is put into mass production.

(10) Selection of Schottky barrier diode



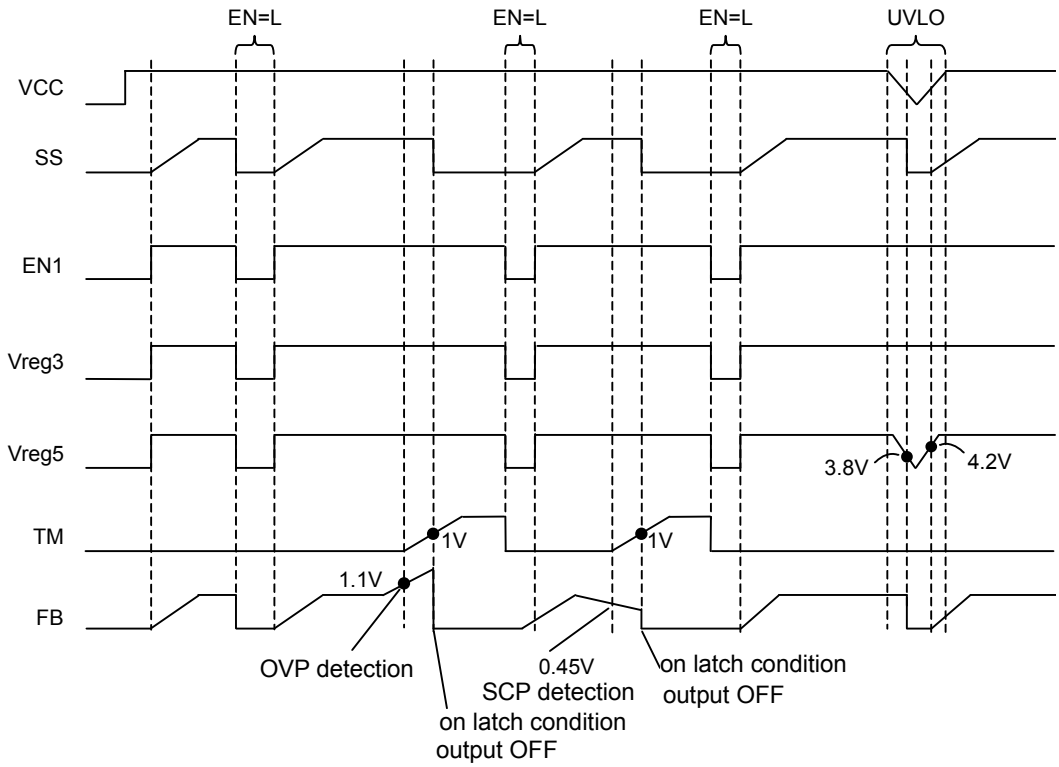
・Reverse breakdown voltage V_R＞Vcc

・Allowable current ＞ output current + ripple current

□ It is recommended to be more that the set value of overcurrent protection

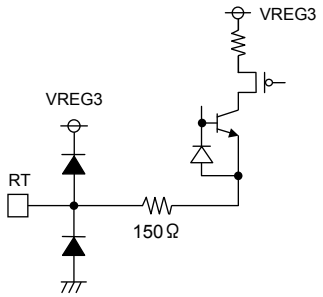
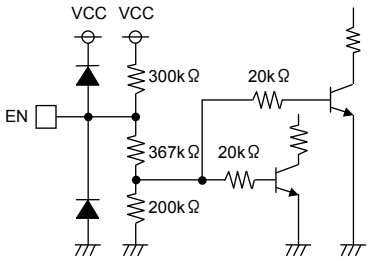
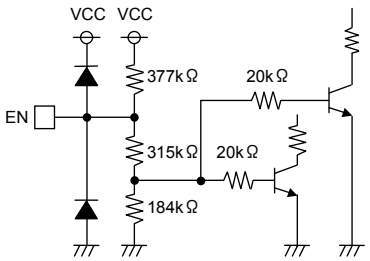
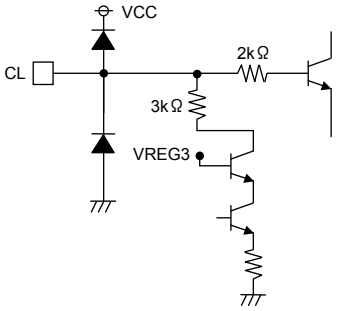
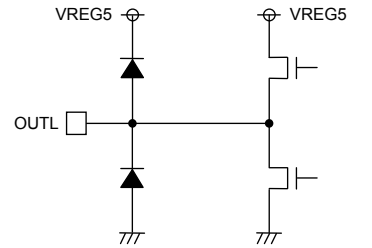
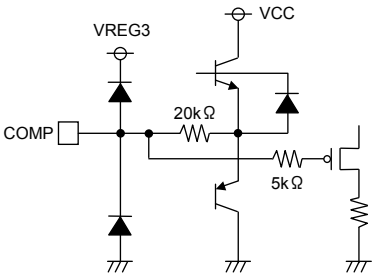
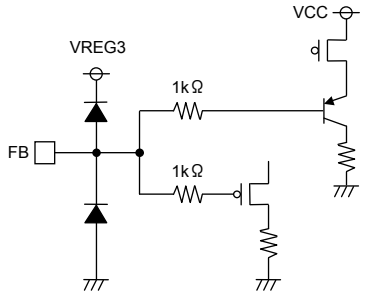
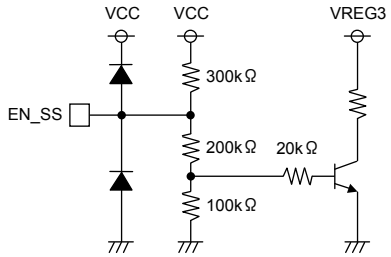
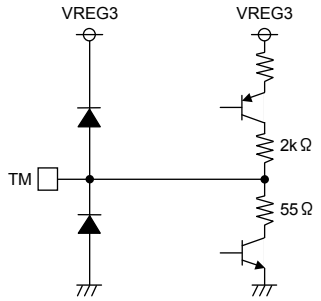
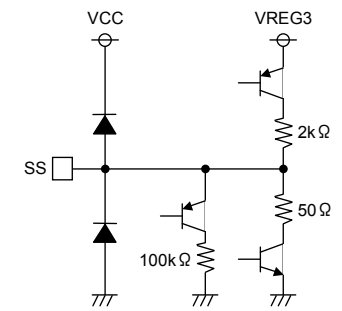
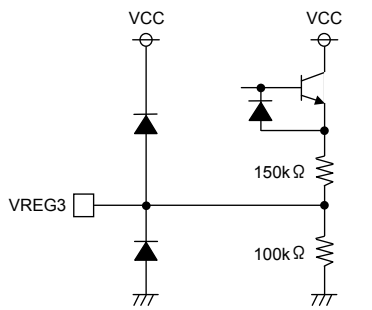
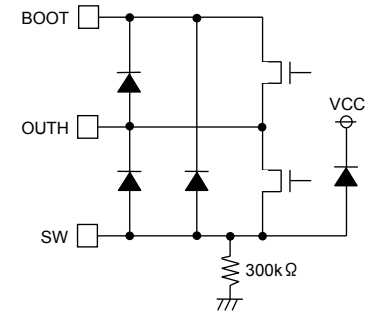
□ High efficiency is obtained if those with small forward voltage and short recovery time (rapid recovery) are selected.

○ Timing chart



● Input & output equivalent circuits

□ The inside of ( ) is of BD9045FV

2(24)PIN [RT]	7 PIN [EN]	(20,22)PIN [EN1, EN2]
		
20PIN [CL] (9,6)PIN [CL1, CL2]	15PIN [OUTL] (14, 1)PIN [OUTL1, OUTL2]	5PIN [COMP] (18,26)PIN [COMP1, COMP2]
		
6 PIN [FB] (19, 25)IN [FB1, FB2]	1 PIN [EN_SS]	3PIN [TM] (6, 28)PIN [TM1, TM2]
		
4PIN [SS] (7, 27)PIN [SS1, SS2]	9PIN [VREG3] (23)PIN [VREG3]	9,17,18PIN [BOOT, SW, OUTH] (10, 5)PIN [BOOT1, BOOT2] (12, 3)PIN [SW1, SW2] (11, 4)PIN [OUTH1, OUTH2]
		

Usage Notes

1. Absolute maximum specification

   If absolute maximum rating such as applied voltage and working temperature range etc. is exceeded, deterioration or breakdown may occur as a result.

   Moreover, such destructive conditions as short mode or open mode etc. can not be assumed. If a particular mode such as exceeding the absolute maximum rating is assumed, please consider taking physical safety measures such as fuse etc.

2. GND electric potential

   Please make the electric potential of GND terminal to be the lowest electric potential under any operating state. In addition, actually including transient phenomenon, please do not make the electrical potentials of all terminals but SW lower than GND's. if there is a terminal, electric potential of which is lower than that of GND, please take such measures as provide a bypass route etc.

3. Permissible dissipation Pd

   If by any chance you use it in such a way that the permissible dissipation is exceeded, occurs the deterioration of original performances of IC such as reduction of current capacity caused by an increase in temperature of chip, which will lead to a decline in reliability, therefore please use it in such a way that its dissipation is within the permissible one with a good margin left.

4. Input power supply

   Please wire and arrange in such a way that, in the wiring pattern and pattern layout, the wiring to the input pin V_{IN} is sufficiently short and furthermore electrical interference is not caused.

   The electrical characteristics included in this specification may vary with such conditions as temperature, power supply voltage and external circuits etc., so please confirm them thoroughly including transient characteristic.

6. Thermal shutdown circuit

   Thermal shutdown circuit is built-in in order to prevent the thermal destruction of IC. Please use it within its permissible dissipation range, but if by any chance the state of exceeding the permissible dissipation continues, the temperature of chip rises, as a result the thermal shutdown circuit operates and so the output is turned off.

   If after that the temperature Tj of chip falls, the circuit resets automatically. Furthermore, the thermal shutdown circuit leads to the state of exceeding the absolute maximum rating, so please absolutely avoid such set design as uses the thermal shutdown circuit.

7. wrong mounting leading to short circuit between pins

   Please be careful of direction and displacement of IC when mounting the printed board. Erroneous mounting may cause the breakdown of IC.

   Moreover, if a foreign body goes in between the outputs or between output & power supply GND and causes a short circuit, there is also a possibility of breakdown.

8. If Vcc and various terminal voltages are in reverse in application, there is a possibility to damage the internal circuit or elements. For example, such case as Vcc is shorted to GND because external capacitor is being charged.

   Please use 1μF and 0.1μF respectively as the capacitor of VREG5's output terminal and the capacitor of VREG3's output terminal. Moreover, it is recommended to insert the backflow-preventing diode in Vcc series or to insert the diode of bypass between various terminals and Vcc.

9. Please be careful that there is a possibility of malfunction which is happening rarely when you use it in a strong electromagnetic field.

10. Please insert the protective diode when it is conceivable that the back electromotive force is produced at the time of start-up or output OFF because a load that has a large inductance component is connected on output terminal.

11. Inspection of set board

    If a capacitor is connected on a pin with low impedance, the IC may be under stress, so please be sure to discharge it once a process at the time of inspection of set board.

    The grounding is carried out at assembly process as a countermeasure against static electricity, so please pay full attention at the time of transportation and preservation. Moreover, please be sure to turn off the power supply before connecting or before detaching when it is connected to jig at inspection process.

12. GND wiring pattern

    If there are both small-signal GND and large-current GND, then large-current GND pattern and small-signal GND pattern are

    separated, and in order that the pattern wiring and the voltage change caused by large current do not change the voltage of

small-signal GND, it is recommended to carry out the one-point grounding at the reference point of set.
Please be careful of not changing the GND wiring pattern of external parts.

13. SW terminal

In case of connecting of application, SW terminal may become a negative electric potential due to the back electromotive force of coil. Please take such measures as provide a bypas route between SW terminal and GND at the time of setting of application.

14. Output

At the time of EN=L, UVLO, and timer latch, the current flows out from SW terminal. If the service condition is such that the output load becomes no more than 1mA, then please insert a 1kΩ resistor between output and GND.

Notes

- No technical content pages of this document may be reproduced in any form or transmitted by any means without prior permission of ROHM CO.,LTD.
- The contents described herein are subject to change without notice. The specifications for the product described in this document are for reference only. Upon actual use, therefore, please request that specifications to be separately delivered.
- Application circuit diagrams and circuit constants contained herein are shown as examples of standard use and operation. Please pay careful attention to the peripheral conditions when designing circuits and deciding upon circuit constants in the set.
- Any data, including, but not limited to application circuit diagrams information, described herein are intended only as illustrations of such devices and not as the specifications for such devices. ROHM CO.,LTD. disclaims any warranty that any use of such devices shall be free from infringement of any third party's intellectual property rights or other proprietary rights, and further, assumes no liability of whatsoever nature in the event of any such infringement, or arising from or connected with or related to the use of such devices.
- Upon the sale of any such devices, other than for buyer's right to use such devices itself, resell or otherwise dispose of the same, no express or implied right or license to practice or commercially exploit any intellectual property rights or other proprietary rights owned or controlled by
- ROHM CO., LTD. is granted to any such buyer.
- Products listed in this document are no antiradiation design.

The products listed in this document are designed to be used with ordinary electronic equipment or devices (such as audio visual equipment, office-automation equipment, communications devices, electrical appliances and electronic toys).
Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
It is our top priority to supply products with the utmost quality and reliability. However, there is always a chance of failure due to unexpected factors. Therefore, please take into account the derating characteristics and allow for sufficient safety features, such as extra margin, anti-flammability, and fail-safe measures when designing in order to prevent possible accidents that may result in bodily harm or fire caused by component failure. ROHM cannot be held responsible for any damages arising from the use of the products under conditions out of the range of the specifications or due to non-compliance with the NOTES specified in this catalog.

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact your nearest sales office.

ROHM Customer Support System

THE AMERICAS / EUROPE / ASIA / JAPAN

www.rohm.com

Contact us : webmaster@rohm.co.jp

ROHM CO., LTD. 21 Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585, Japan
TEL : +81-75-311-2121
FAX : +81-75-315-0172